ALPHA & OMEGA SEMICONDUCTOR

AOD609G

Complementary Enhancement Mode Field Effect Transistor

General Description

The AOD609G uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

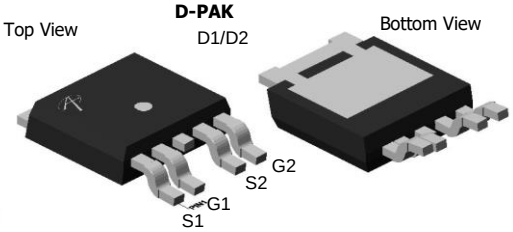
-RoHS Compliant
-Halogen Free*

Features

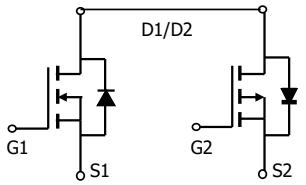
n-channel
V_{DS} (V) = 40V, I_D = 12A (V_{GS}=10V)
$R_{DS(ON)}$< 30mΩ (V_{GS}=10V)
$R_{DS(ON)}$< 40mΩ (V_{GS}=4.5V)
p-channel
V_{DS} (V) = -40V, I_D = -12A (V_{GS}=-10V)
$R_{DS(ON)}$< 45mΩ (VGS= -10V)
$R_{DS(ON)}$< 66mΩ (VGS= -4.5V)
100% UIS Tested!
100% Rg Tested!

Green Product RoHS Compliant

TO-252-4L
D-PAK



Top View
Drain Connected to Tab



n-channel **p-channel**

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current [B,G]	T_C=25°C	I_D	12	-12	A
	T_C=100°C		12	-12	
Pulsed Drain Current [B]		I_{DM}	30	-30	
Avalanche Current [C]		I_{AR}	14	-20	
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	9.8	20	mJ
Power Dissipation	T_C=25°C	P_D	27	30	W
	T_C=100°C		14	15	
Power Dissipation	T_A=25°C	P_{DSM}	2	2	W
	T_A=70°C		1.3	1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	-55 to 175	°C

Thermal Characteristics: n-channel and p-channel

Parameter		Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient [A,D]	t ≤ 10s	$R_{\theta JA}$	n-ch	17.4	25	°C/W
Maximum Junction-to-Ambient [A,D]	Steady-State		n-ch	50	60	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	n-ch	4	5.5	°C/W
Maximum Junction-to-Ambient [A,D]	t ≤ 10s	$R_{\theta JA}$	p-ch	16.7	25	°C/W
Maximum Junction-to-Ambient [A,D]	Steady-State		p-ch	50	60	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	p-ch	3.5	5	°C/W

N Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.7	2.5	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=12A		24	30	mΩ
		T_J=125°C		37	46	
		V_{GS}=4.5V, I_D=8A		31	40	
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=12A		25		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz		545		pF
C_{oss}	Output Capacitance			65		pF
C_{rss}	Reverse Transfer Capacitance			40		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1.6	3.2	4.8	Ω
SWITCHING PARAMETERS						
Q_g (10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=12A		10	13	nC
Q_{gs}	Gate Source Charge			2		nC
Q_{gd}	Gate Drain Charge			2.2		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=20V, R_L=1.4Ω, R_{GEN}=3Ω		5.5		ns
t_r	Turn-On Rise Time			3		ns
$t_{D(off)}$	Turn-Off DelayTime			19		ns
t_f	Turn-Off Fall Time			4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=12A, dI/dt=100A/µs		13		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=12A, dI/dt=100A/µs		6.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=175° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.
*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D= -250µA, V_{GS}=0V	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= -40V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D= -250µA	-1.7	-2	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}= -10V, V_{DS}= -5V	-30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}= -10V, I_D= -12A		36	45	mΩ
		T_J=125°C		52	65	
		V_{GS}= -4.5V, I_D= -8A		51	66	
g_{FS}	Forward Transconductance	V_{DS}= -5V, I_D= -12A		22		S
V_{SD}	Diode Forward Voltage	I_S= -1A,V_{GS}=0V		-0.76	-1	V
I_S	Maximum Body-Diode Continuous Current				-12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}= -20V, f=1MHz		890		pF
C_{oss}	Output Capacitance			90		pF
C_{rss}	Reverse Transfer Capacitance			60		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	6.5	13	19.5	Ω
SWITCHING PARAMETERS						
Q_g (-10V)	Total Gate Charge	V_{GS}= -10V, V_{DS}= -20V, I_D= -12A		15.5	21	nC
Q_g (-4.5V)	Total Gate Charge			7	9	nC
Q_{gs}	Gate Source Charge			3.2		nC
Q_{gd}	Gate Drain Charge			3.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}= -10V, V_{DS}= -20V, R_L=1.4Ω, R_{GEN}=3Ω		10		ns
t_r	Turn-On Rise Time			15.5		ns
$t_{D(off)}$	Turn-Off DelayTime			35		ns
t_f	Turn-Off Fall Time			50		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F= -12A, dI/dt=100A/µs		20		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F= -12A, dI/dt=100A/µs		11		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=175° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.
*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

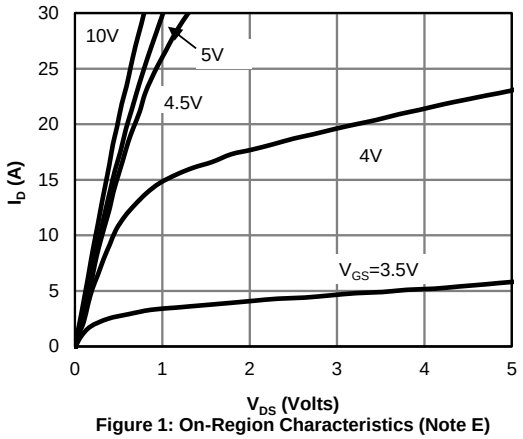


Figure 1: On-Region Characteristics (Note E)

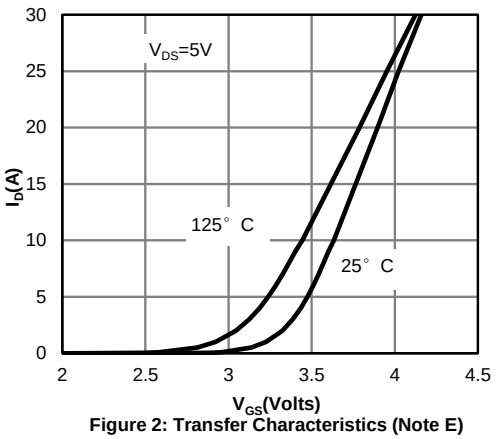


Figure 2: Transfer Characteristics (Note E)

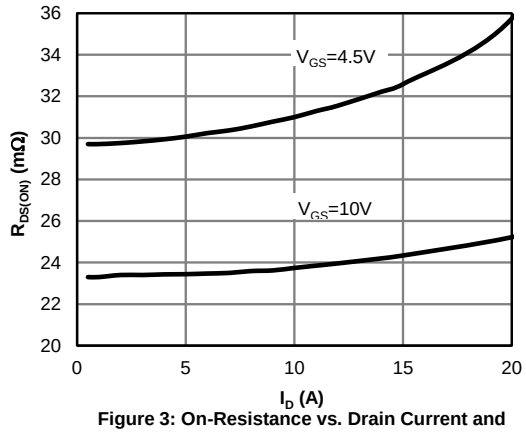


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

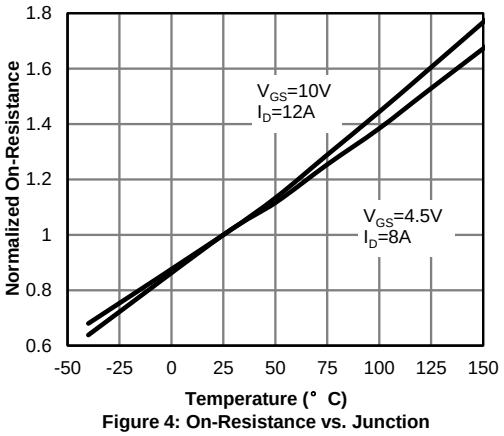


Figure 4: On-Resistance vs. Junction Temperature (Note E)

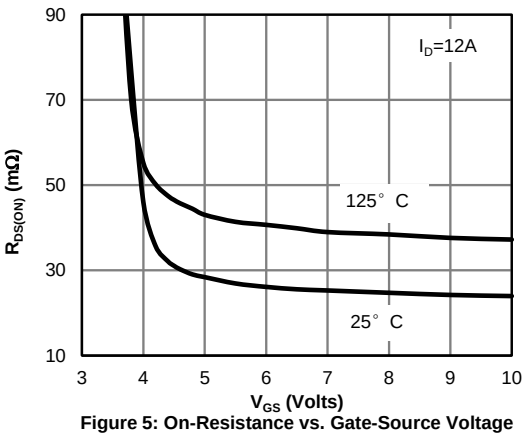


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

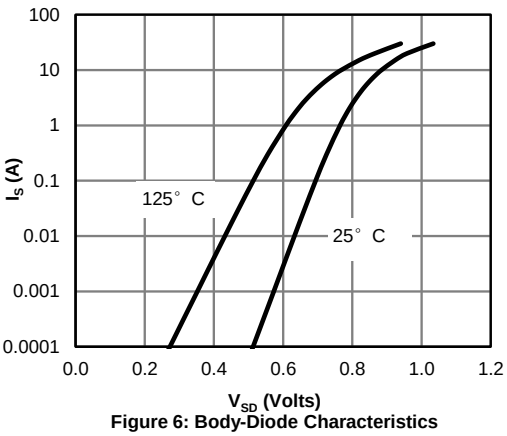


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

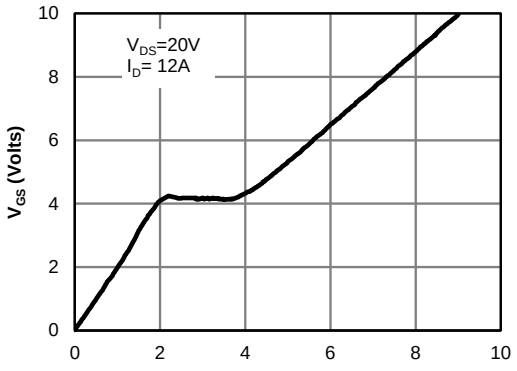


Figure 7: Gate-Charge Characteristics

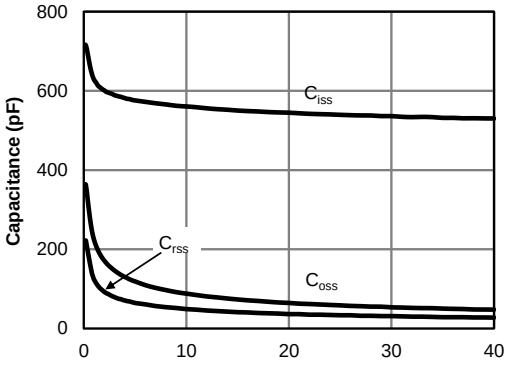


Figure 8: Capacitance Characteristics

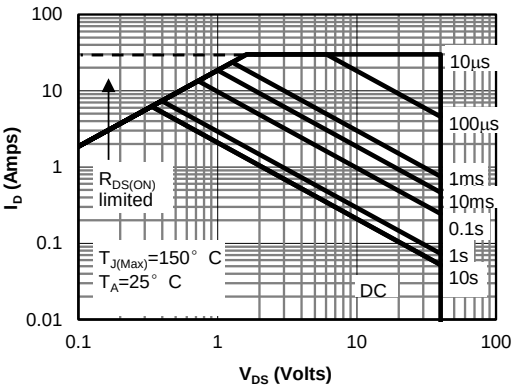


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

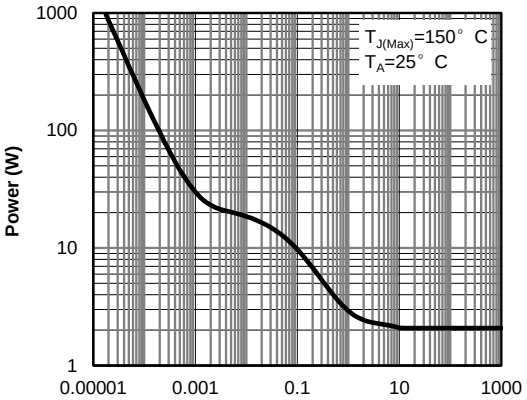


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)

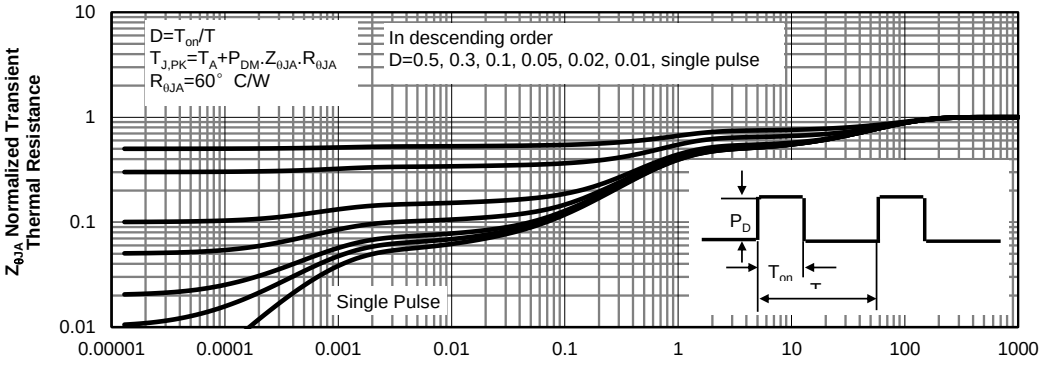
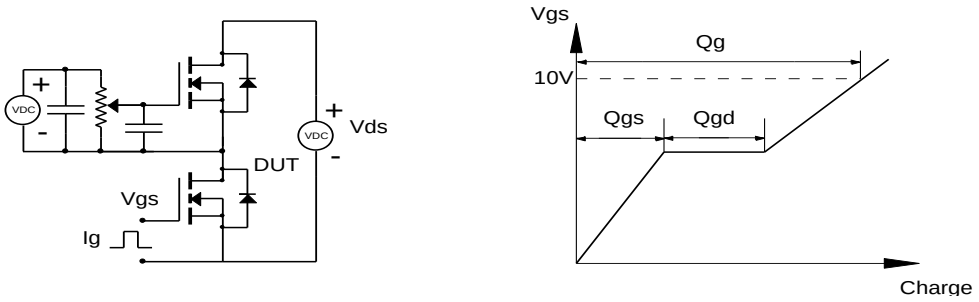


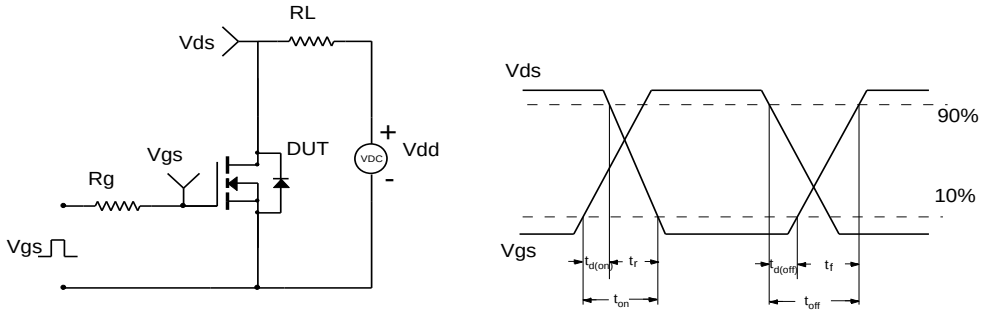
Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)

TEST CIRCUTS AND WAVEFORMS: N-CHANNEL

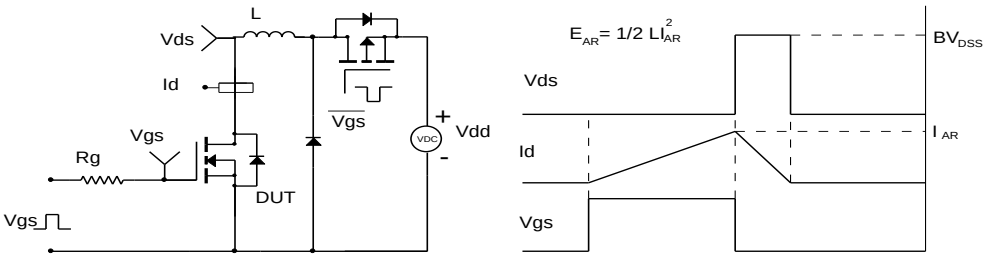
Gate Charge Test Circuit & Waveform



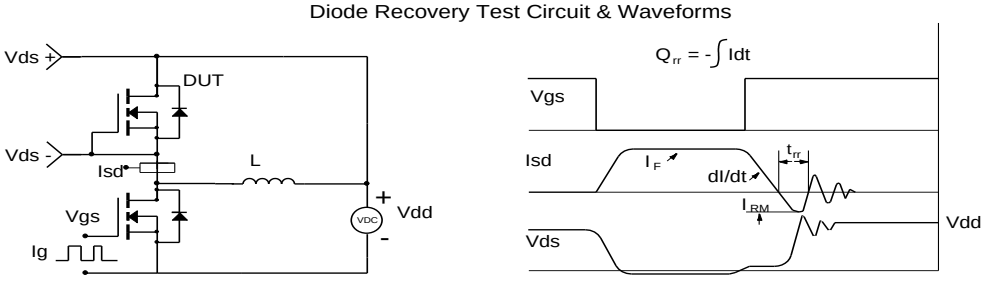
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

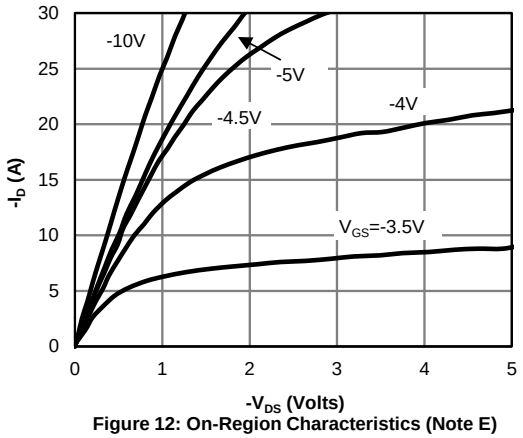


Figure 12: On-Region Characteristics (Note E)

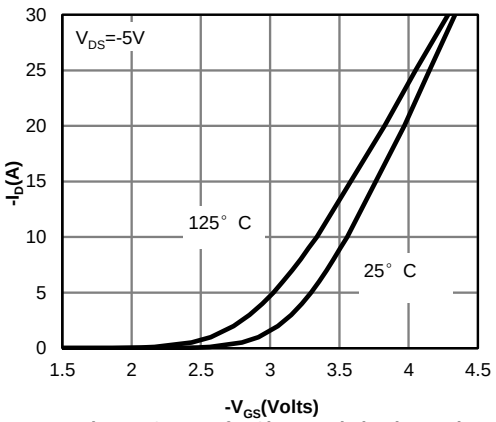


Figure 13: Transfer Characteristics (Note E)

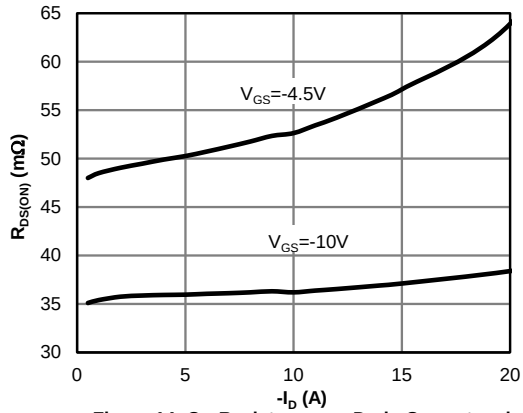


Figure 14: On-Resistance vs. Drain Current and Gate Voltage (Note E)

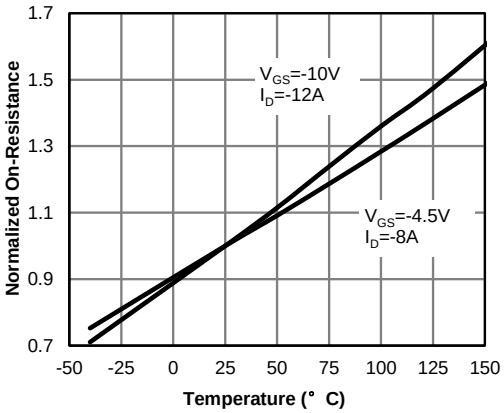


Figure 15: On-Resistance vs. Junction Temperature (Note E)

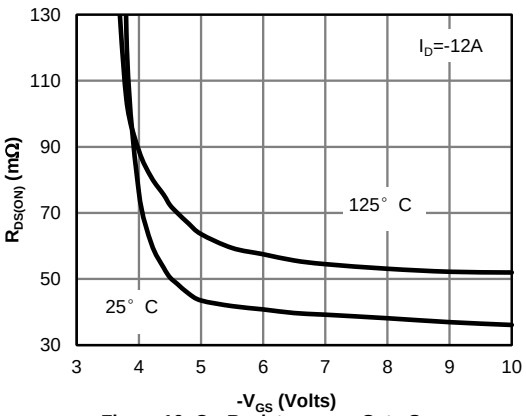


Figure 16: On-Resistance vs. Gate-Source Voltage (Note E)

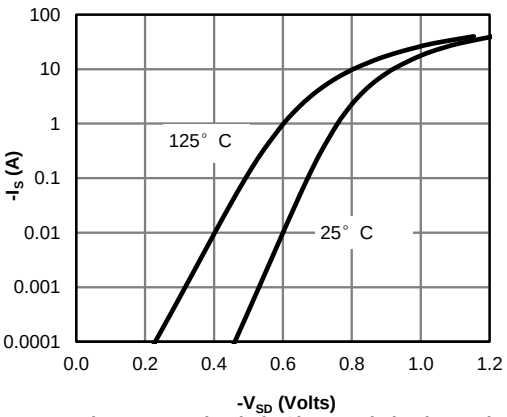


Figure 17: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

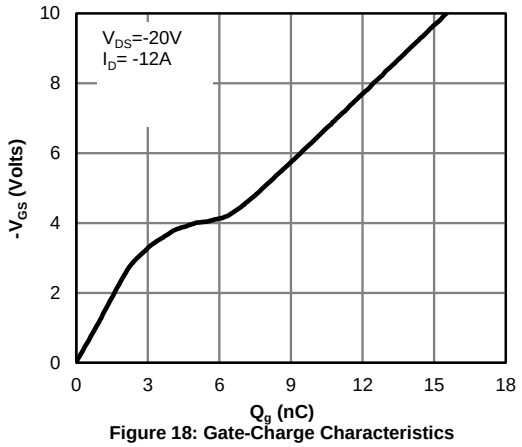


Figure 18: Gate-Charge Characteristics

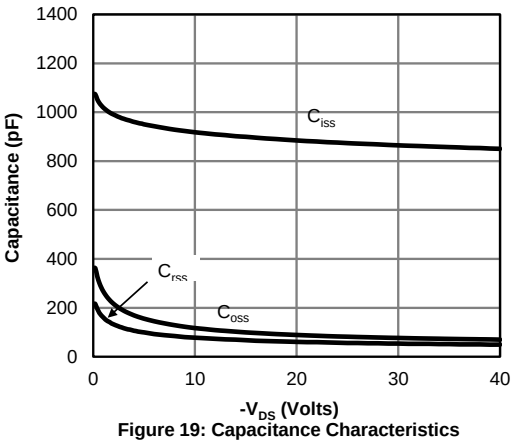


Figure 19: Capacitance Characteristics

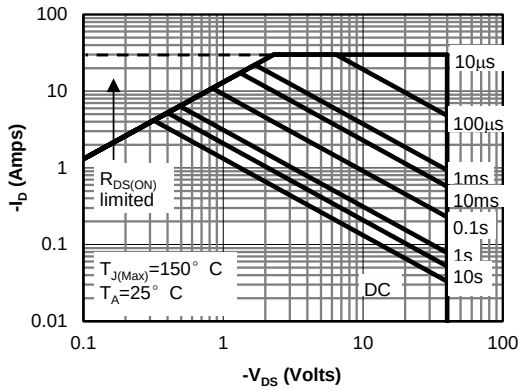


Figure 20: Maximum Forward Biased Safe Operating Area (Note F)

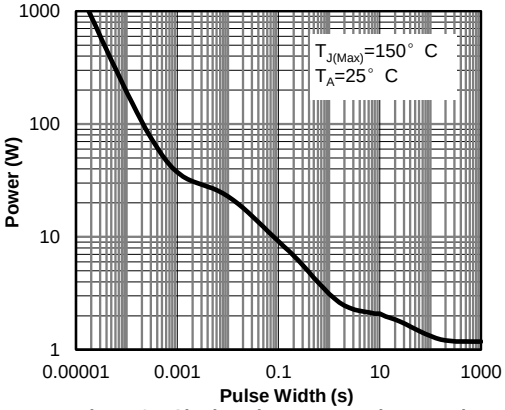


Figure 21: Single Pulse Power Rating Junction-to-Ambient (Note H)

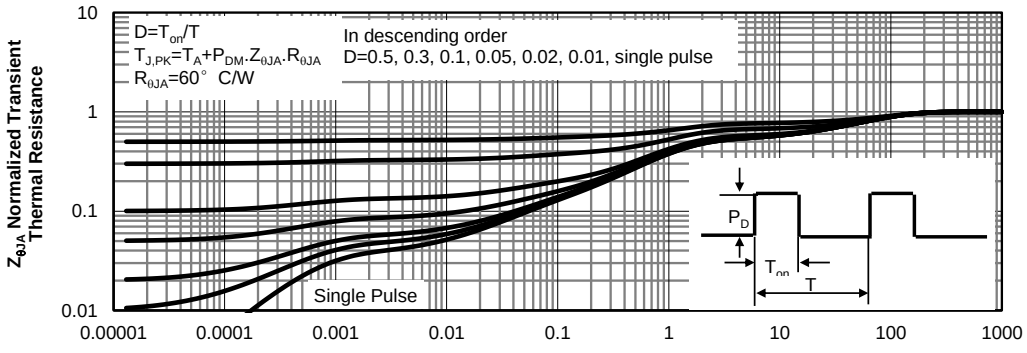
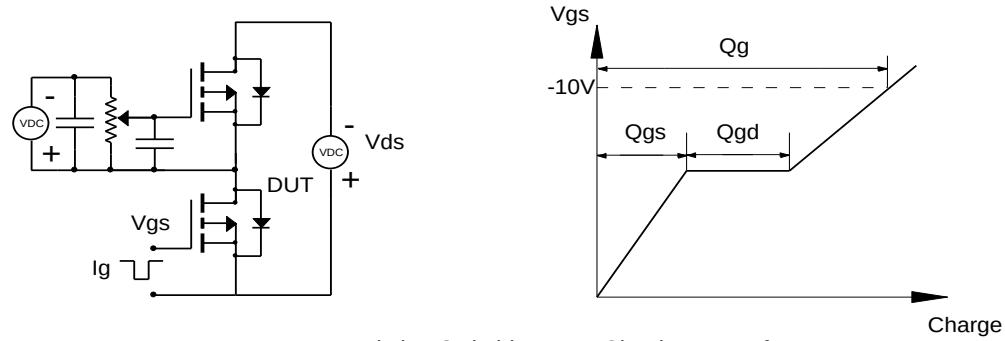


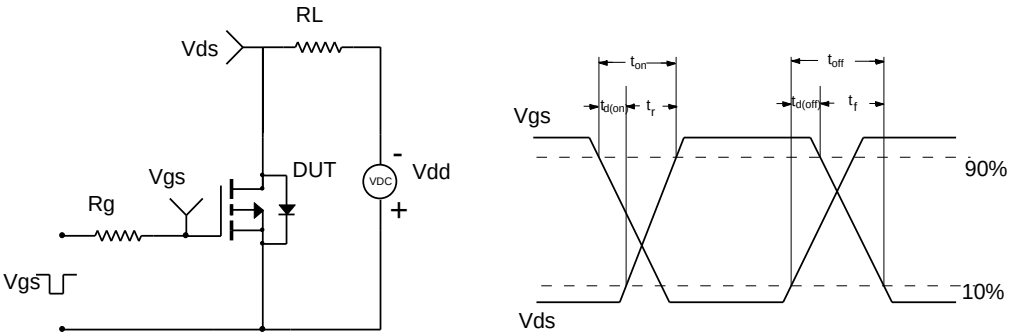
Figure 22: Normalized Maximum Transient Thermal Impedance (Note H)

TEST CIRCUTS AND WAVEFORMS: P-CHANNEL

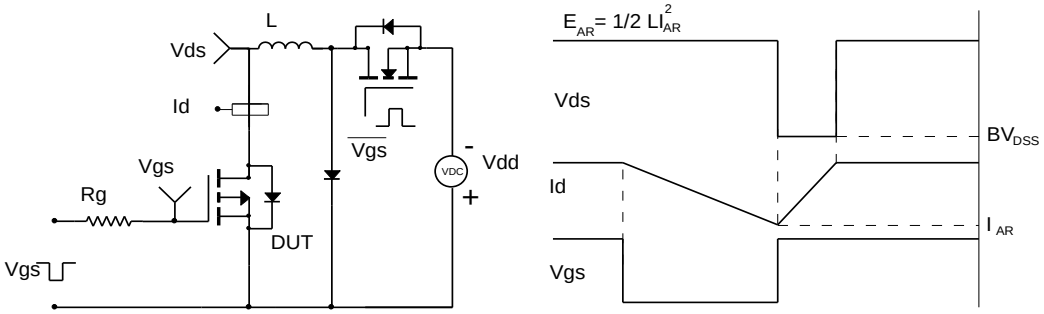
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms